

## QSFP-DD 400G AOC 850nm

### AD85S24-CP-XXX

#### FEATURES

- Hot Pluggable QSFP-DD form factor
- QSFP-DD MSA compliant
- IEEE 802.3bs 400GAUI-8 standard compliant
- Digital diagnostic functions
- Non-Hermetic package design
- Support 425Gb/s aggregate bit rate
- 8x50G PAM4 VCSEL/PIN photo detector
- Maximum power consumption < 11W each end
- Operating case temperature: 0°C~70°C
- RoHS-6: Environment Safety

#### APPLICATIONS

- 400GE Ethernet
- Data Center Network

#### ORDERING INFORMATION

Part Number	Form Factor	Data Rate	Media	Distance (m)	Wavelength (nm)	Temperature (°C)
AD85S24-CP-XXX	QSFP-DD	400G	MMF	-	850	0~70

#### 1 ABSOLUTE MAXIMUM PARAMETERS

Exceeding the limits below may damage the active optical cable permanently.

Parameter	Symbol	Min.	Max.	Unit.
Maximum Supply Voltage	Vcc	-0.5	3.6	V
Storage Temperature	Ts	-40	85	°C

Operating Case Temperature	T <sub>c</sub>	0	70	°C
Relative Humidity	Rh	0	85	%

## 2 . OPERATING ENVIRONMENTS

Parameter	Symbol	Min.	Typ.	Max.	Unit.
Case Temperature	T <sub>op</sub>	0		70	°C
Supply Voltage	V <sub>cc</sub>	3.135		3.465	V
Power Consumption	P <sub>con</sub>		10	12	W
Data rate, per lane			26.5 625		GBd
Data rate accuracy		-100		100	ppm
Bit Error Ratio	BER	1E-6			
Modulation format		PAM4			
Center wavelength	λ <sub>c</sub>	840		860	nm
Number of Lanes		16			
Management Interface		Serial, I2C-based, maximum frequency 400 kHz			

## 3 . ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Module Supply Current			3100		mA	
Transceiver Power On Initialization Time				2000	ms	
AC common-mode output voltage(RMS)				17.5	mV	
Differential peak-to-peak output voltage (Transmitter disabled)				35	mV	
Differential peak-to-peak output voltage (Transmitter enabled)				880	mV	
Eye symmetry mask width			0.22		UI	
Eye height, differential		32			mV	

Differential output return loss		See Eq. 1			V	
Common to differential mode conversion return loss		See Eq. 2			V	
Common mode voltage		-350		2850	mV	
Transmission time		10			ps	
Differential Termination Resistance Mismatch		10			%	
Far-end Eye height, differential		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss		See Eq. 1				
Common to differential mode conversion return loss		See Eq. 2				
Differential Termination Mismatch		10			%	
Transmission time		10			ps	20%~80%
DC common mode voltage		-350		2850	mV	TP1

#### 4 . PIN DESCRIPTIONS

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	VccRx	+3.3V Power Supply	2
11	SCL	2-wire Serial Interface Clock	
12	SDA	2-wire Serial Interface Data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	

16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	VccTx	+3.3V Power Supply	2
30	Vcc1	+3.3V Power Supply	2
31	LPMODE	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1
39	GND	Ground	1
40	Tx6n	Transmitter Inverted Data Input	
41	Tx6p	Transmitter Non-Inverted Data Input	
42	GND	Ground	1
43	Tx8n	Transmitter Inverted Data Input	
44	Tx8p	Transmitter Non-Inverted Data Input	
45	GND	Ground	1
46	Reserved	For future use, No Connect	3
47	VS1	Module Vendor Specific 1, No Connect	3
48	VccRx1	+3.3V Power supply	2
49	VS2	Module Vendor Specific 2	3
50	VS3	Module Vendor Specific 3	3
51	GND	Ground	1
52	Rx7p	Receiver Non-Inverted Data Output	

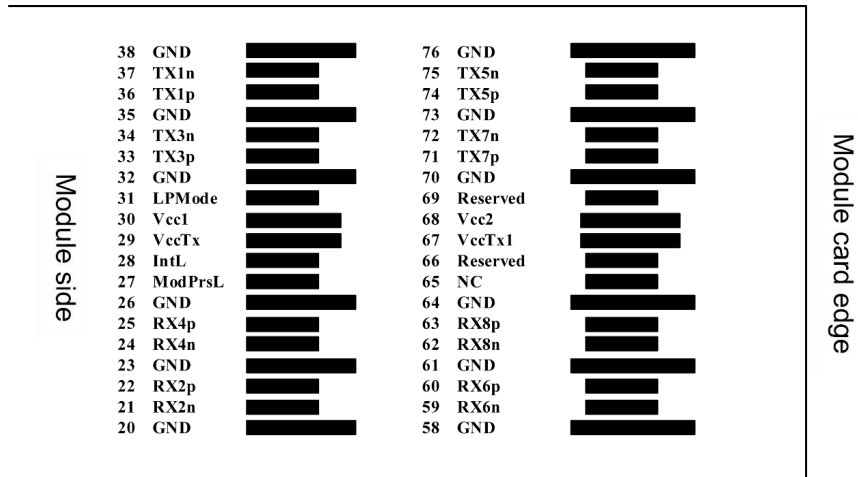
53	Rx7n	Receiver Inverted Data Output	
54	GND	Ground	1
55	Rx5p	Receiver Non-Inverted Data Output	
56	Rx5n	Receiver Inverted Data Output	
57	GND	Ground	1
58	GND	Ground	1
59	Rx6n	Receiver Inverted Data Output	
60	Rx6p	Receiver Non-Inverted Data Output	
61	GND	Ground	1
62	Rx8n	Receiver Inverted Data Output	
63	Rx8p	Receiver Non-Inverted Data Output	
64	GND	Ground	1
65	NC	No Connect	
66	Reserved	For future use, No Connect	
67	VccTx1	+3.3V Power supply	2
68	Vcc2	+3.3V Power supply	2
69	Reserved	For future use, No Connect	
70	GND	Ground	1
71	Tx7p	Transmitter Non-Inverted Data Input	
72	Tx7n	Transmitter Inverted Data Input	
73	GND	Ground	1
74	Tx5p	Transmitter Non-Inverted Data Input	
75	Tx5n	Transmitter Inverted Data Input	
76	GND	Ground	1

**Notes:**

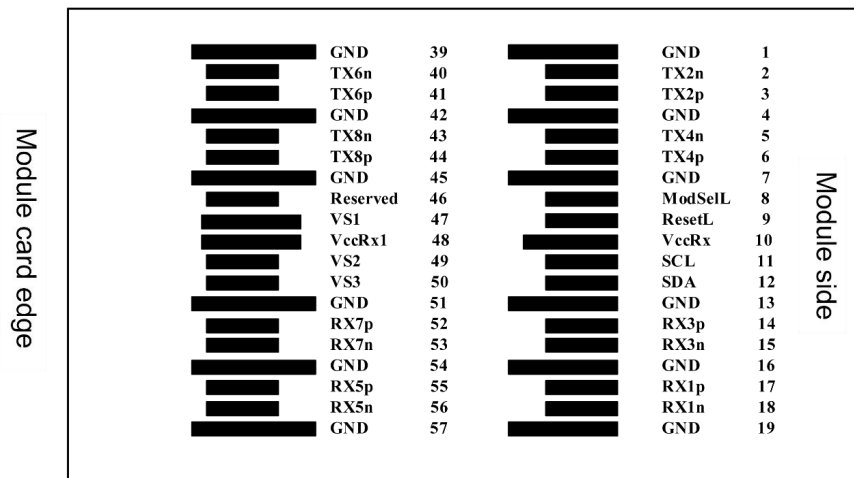
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane

2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in the table. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA

## 5. PIN DIAGRAM

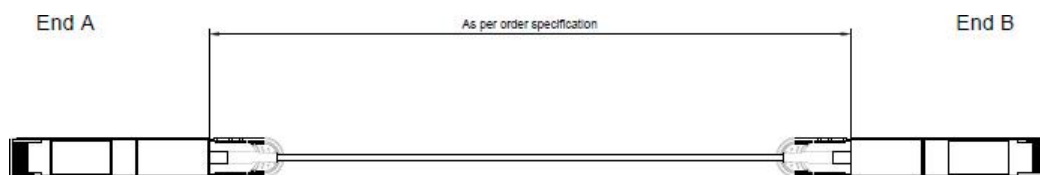


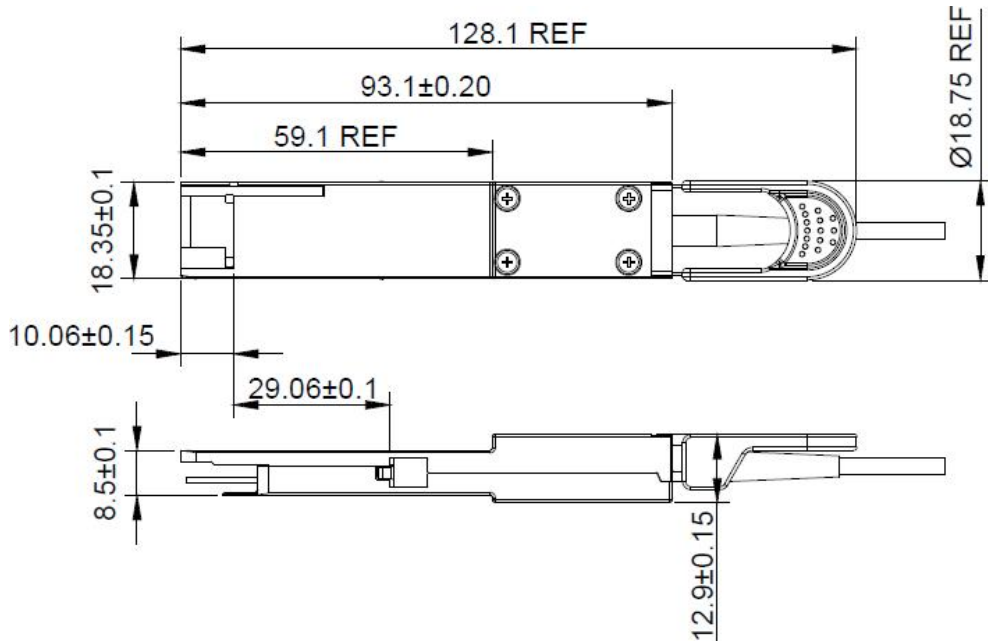
Top side viewed from top



Bottom side viewed from bottom

## 6 . Mechanical Design Diagram





**7 . LABEL DIAGRAM**

Optowire **AD85S24-CP-XXX**

QSFP-DD 400G AOC 850nm

Class 1 Laser  
MADE IN CHINA

S/N: ??????????  




X.XX.XX.XXX